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- (54) **AMBIPOLAR SILICON NANOWIRE FIELD EFFECT TRANSISTOR**
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USPC ..... 257/29, 40, 330–350, 43, 295, 314, 14, 257/E29.082, E29.084, E29.089, E29.255, 257/E21.09, E29.068, E21.409, 257/E21.618–E21.636; 438/149–258, 478, 438/287; 977/937, 720–723, 701, 888, 755, 977/938, 940

See application file for complete search history.

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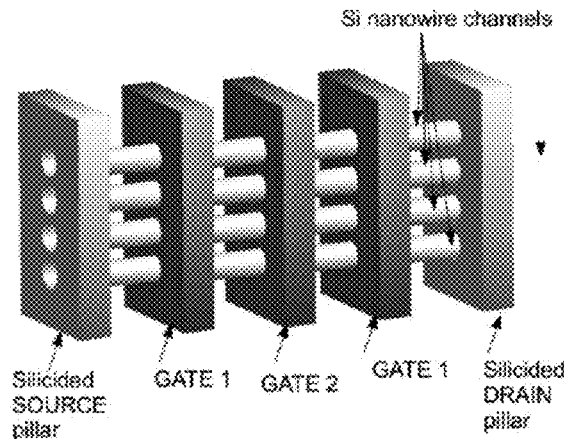
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**H01L 21/00** (2006.01)  
**H01L 21/32** (2006.01)  
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CPC ..... H01L 29/775; H01L 29/66439; H01L 29/408; H01L 29/606; H01L 29/0673; H01L 21/33

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(57) **ABSTRACT**

This invention describes a novel electronic device consisting of one—or more—vertically stacked gate-all-around silicon nanowire field effect transistor (SNWFET) with two independent gate electrodes. One of the two gate electrodes, acting on the central section of the transistor channel, controls on/off behavior of the channel. The second gate, acting on the regions in proximity to the source and the drain of the transistor, defines the polarity of the devices, i.e. p or n type. The electric field of the second gate acts either at the interface of the nanowire-to-source/drain region or anywhere in close proximity to the depleted region of the SiNW body, modulating the bending of the Schottky barriers at the contacts, eventually screening one type of charge carrier to pass through the channel of the transistor. This is achieved by controlling the majority carriers passing through the transistor channel by regulating the Schottky barrier thicknesses at the source and drain contacts.

**12 Claims, 13 Drawing Sheets**



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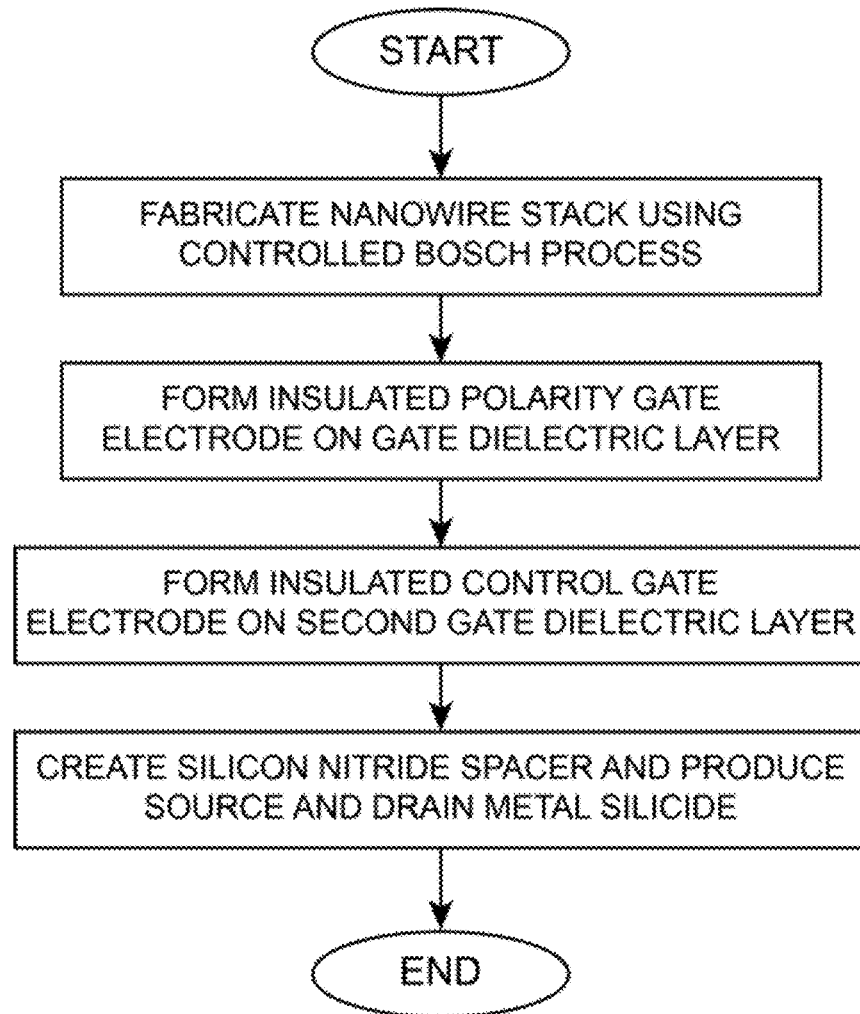


Fig. 1A

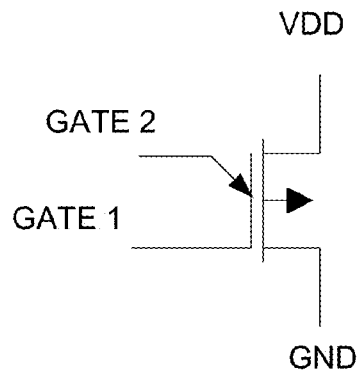


Fig. 1B

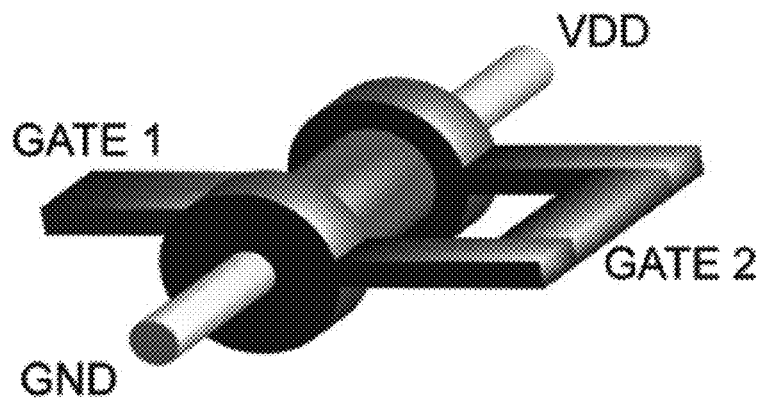


Fig. 1C

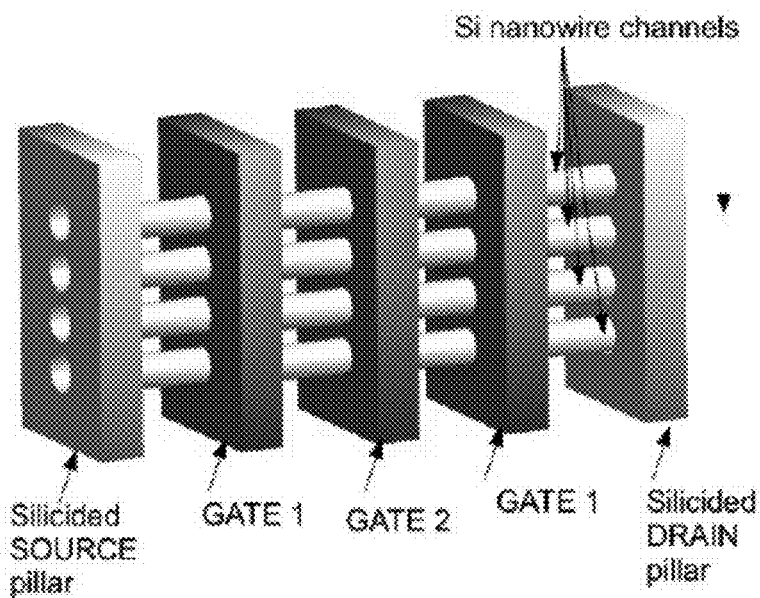


Fig. 1D

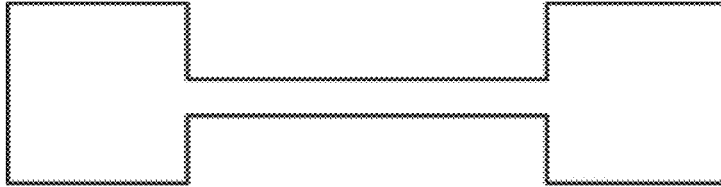


Fig. 2A

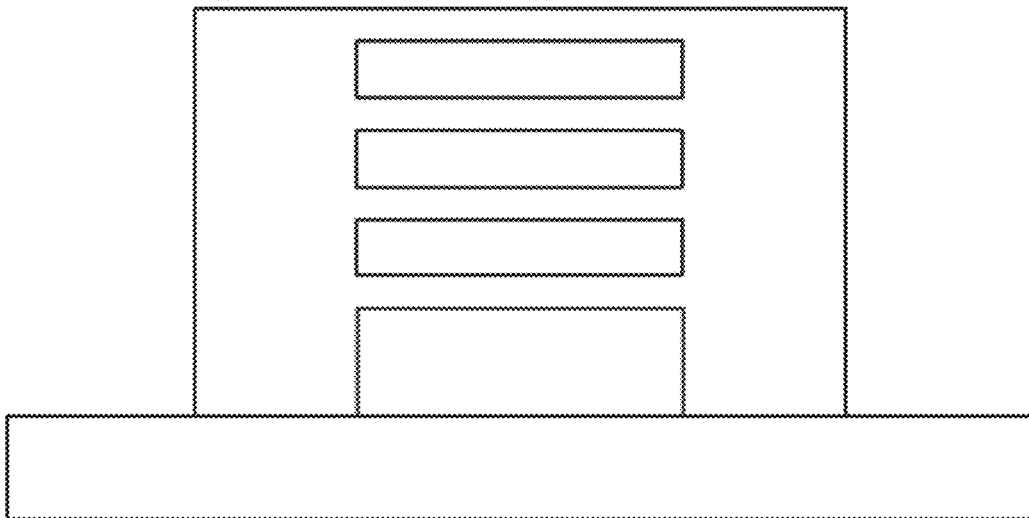


Fig. 2B

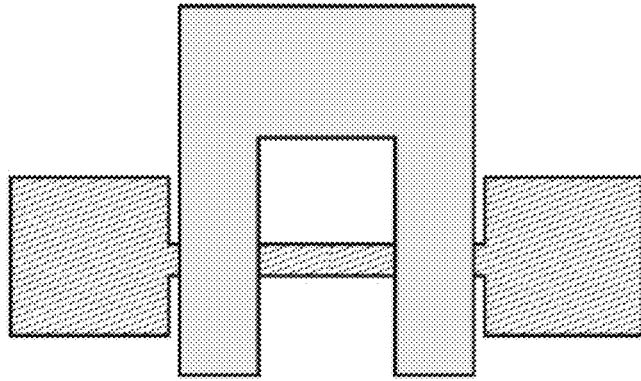


Fig. 2C

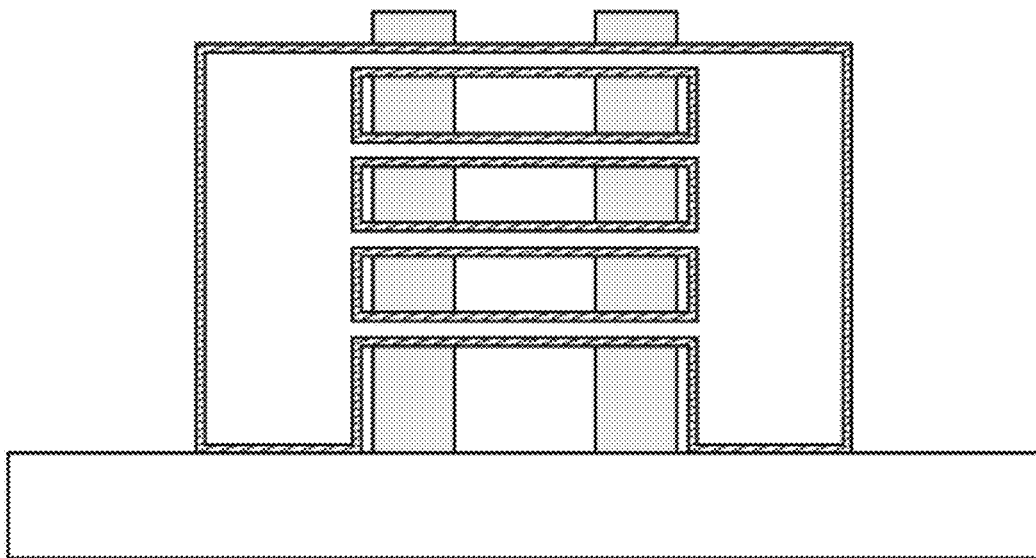


Fig. 2D

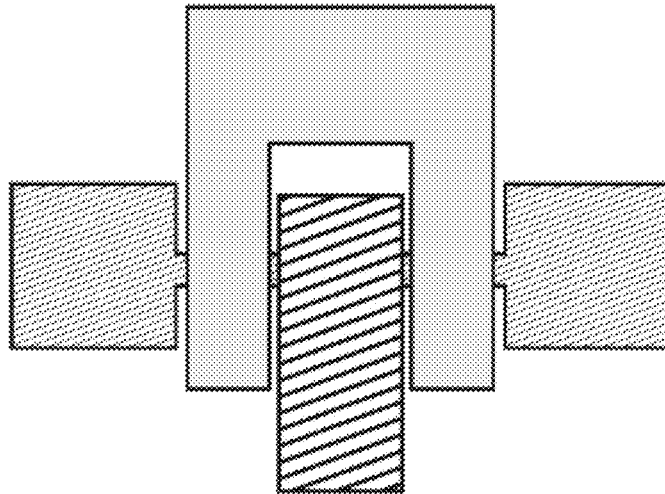


Fig. 2E

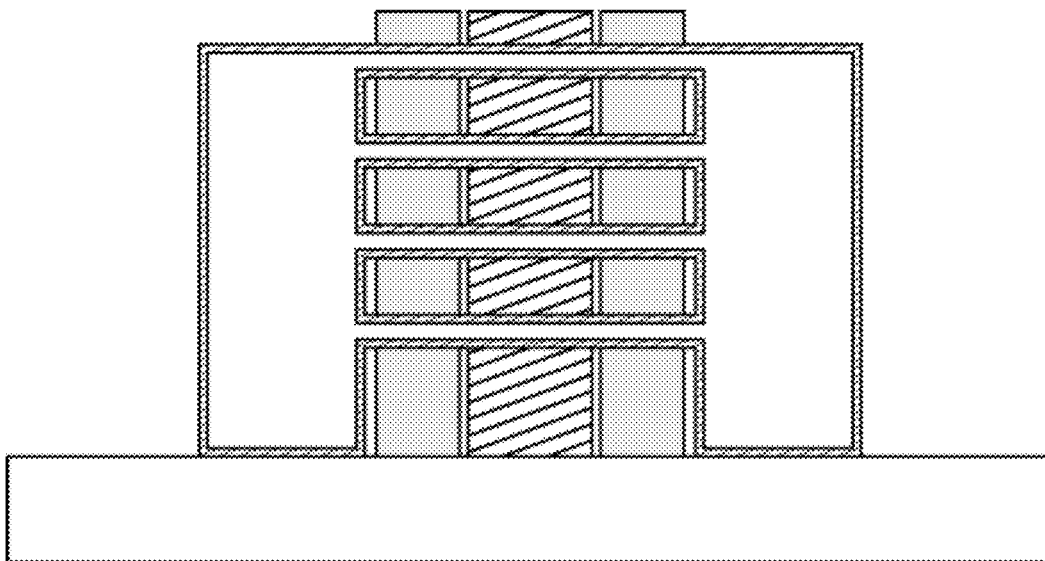


Fig. 2F

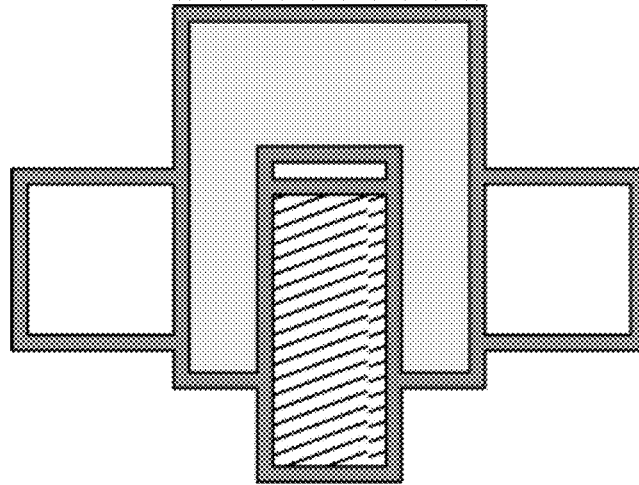


Fig. 2G

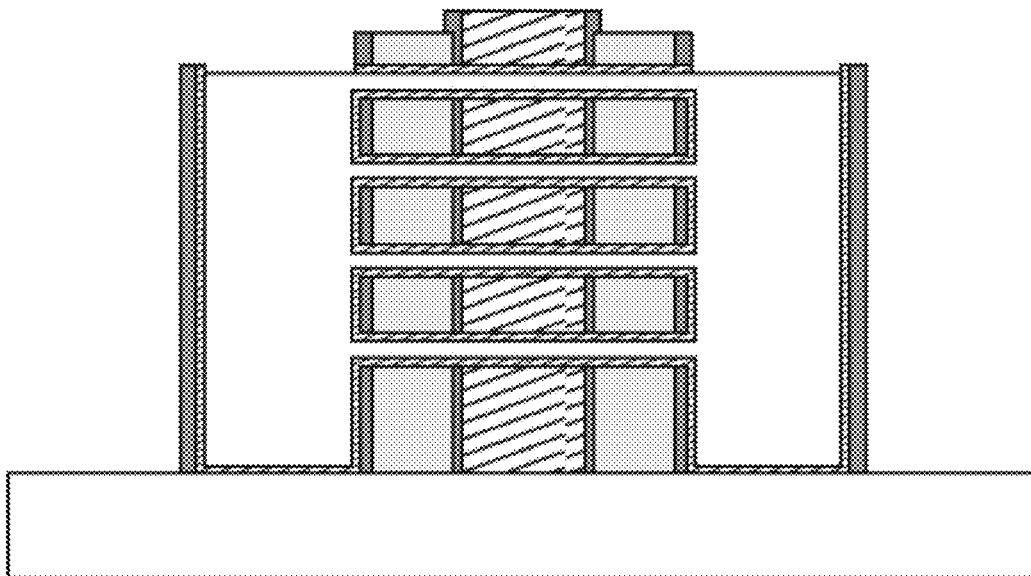


Fig. 2H



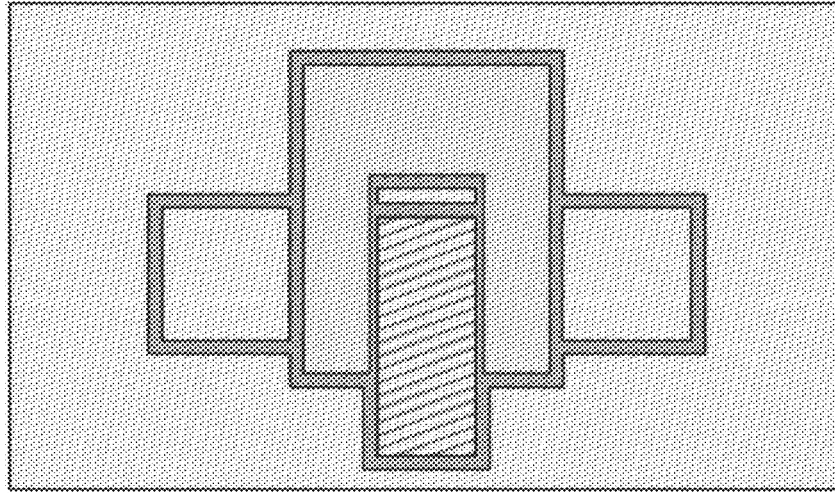


Fig. 2I

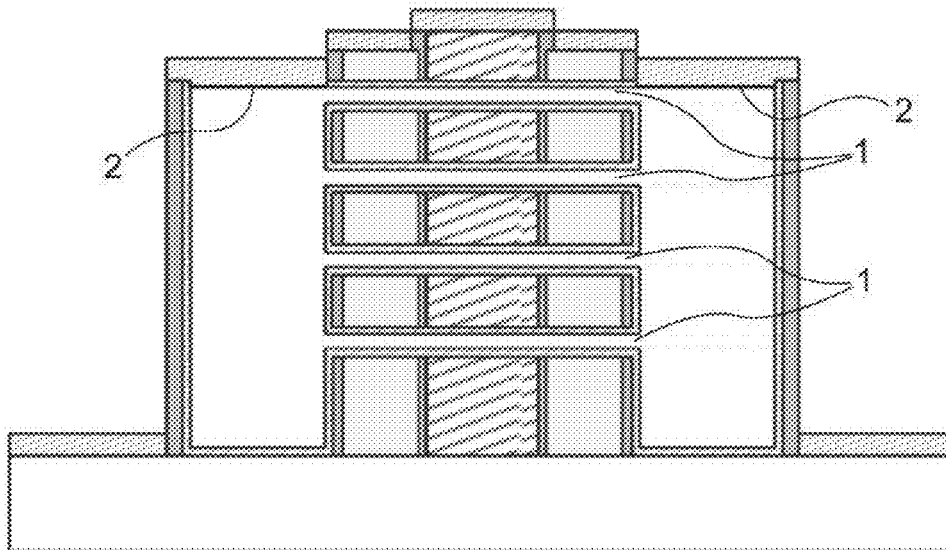


Fig. 2J

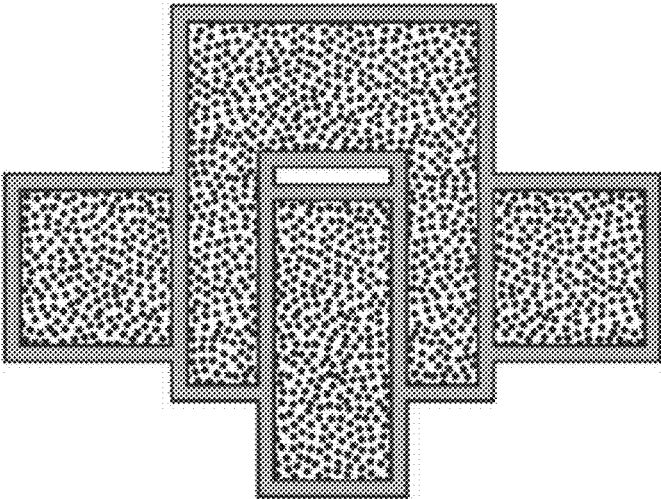


Fig. 2K

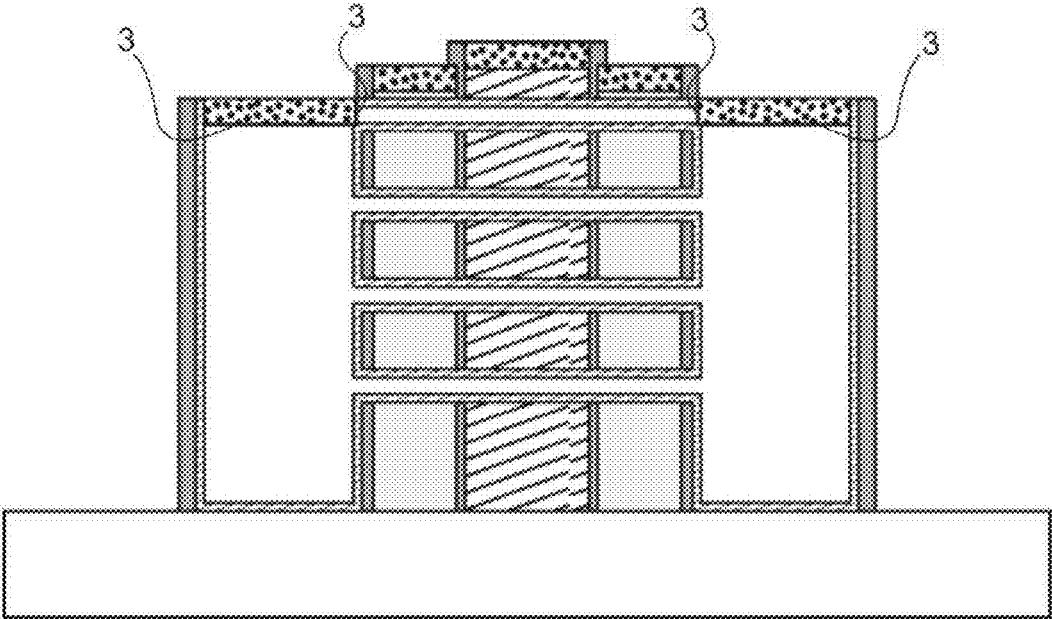


Fig. 2L

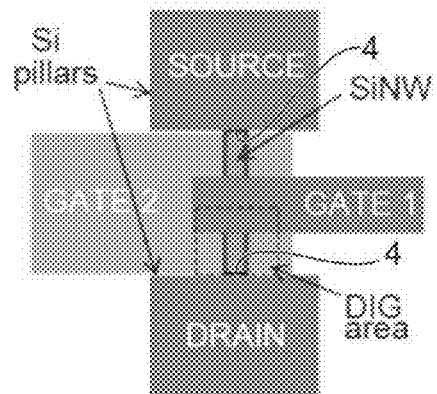


Fig. 3A

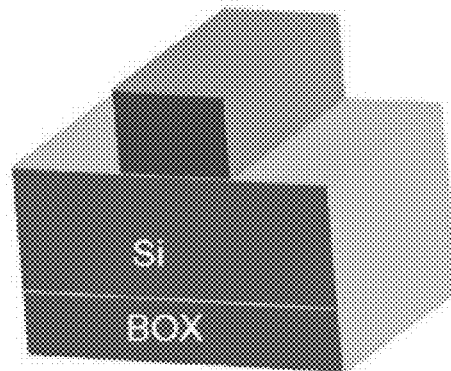


Fig. 3B

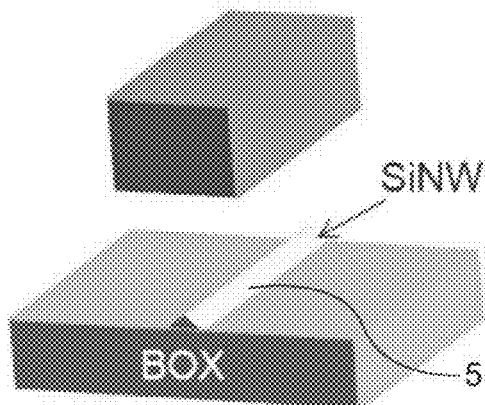


Fig. 3C

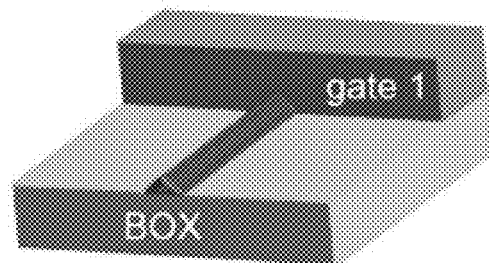


Fig. 3D

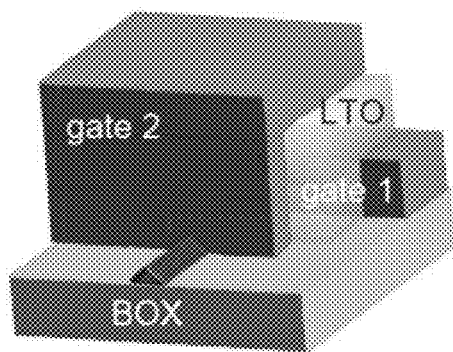


Fig. 3E

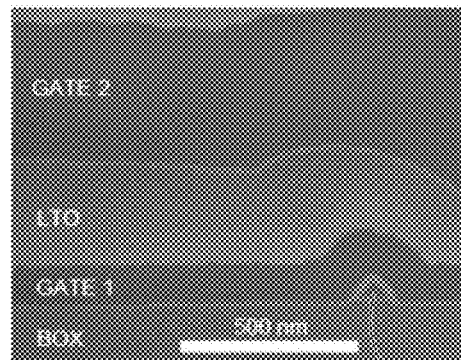


Fig. 3F

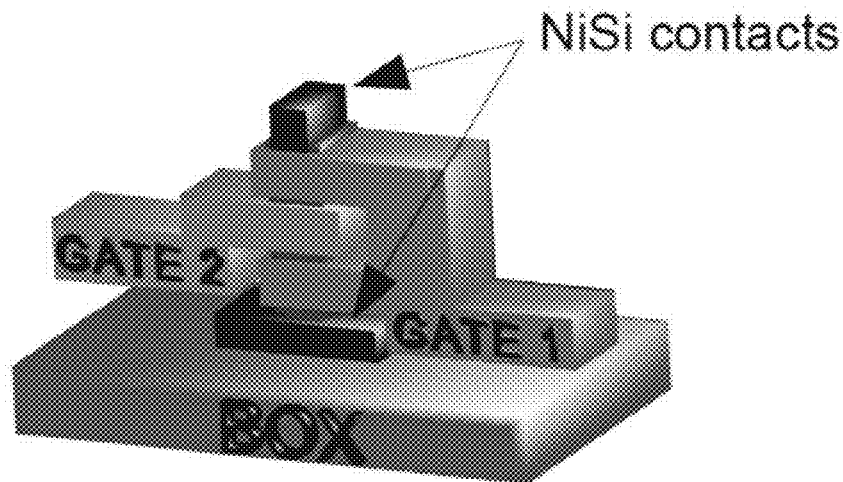


Fig. 4A

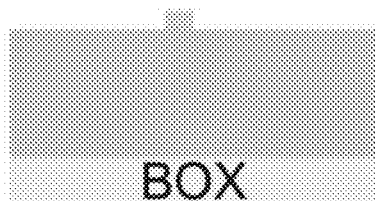


Fig. 4B

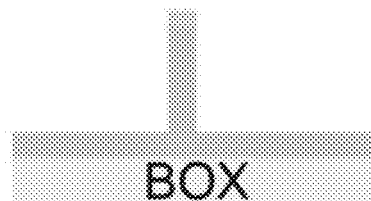


Fig. 4C

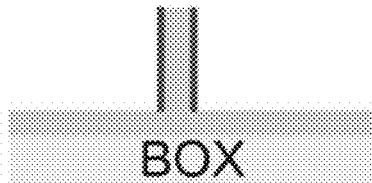


Fig. 4D

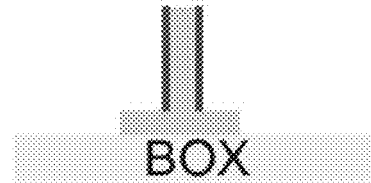


Fig. 4E

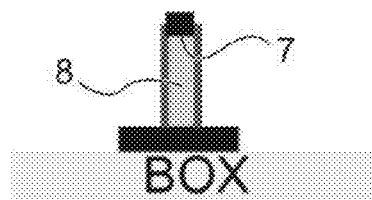


Fig. 4F

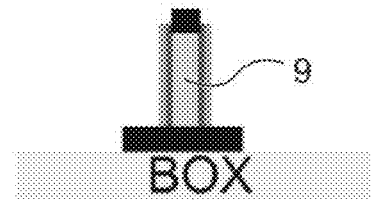


Fig. 4G

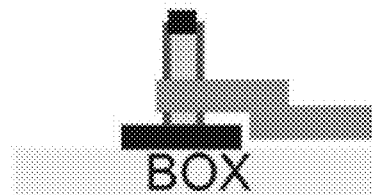


Fig. 4H

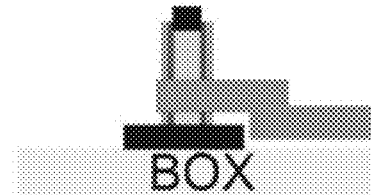


Fig. 4I

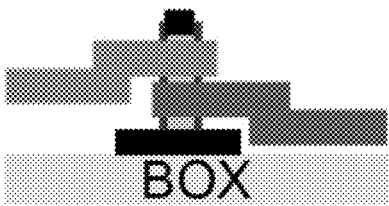


Fig. 4J

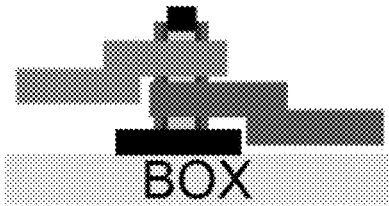


Fig. 4K

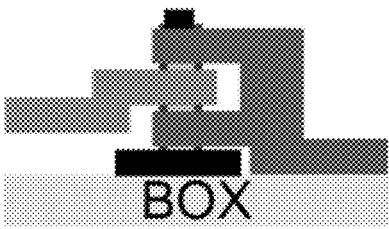


Fig. 4L

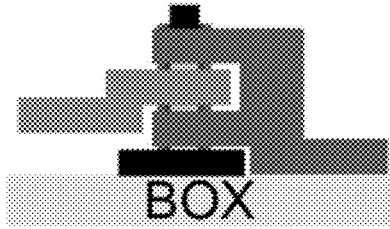


Fig. 4M

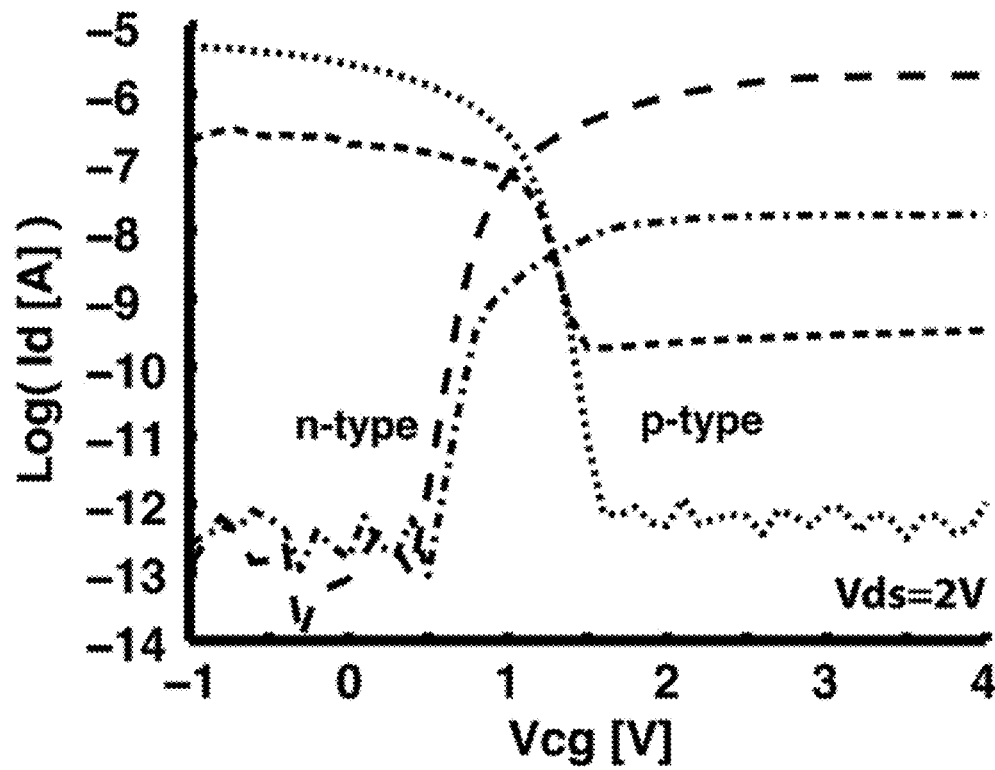


Fig. 5A

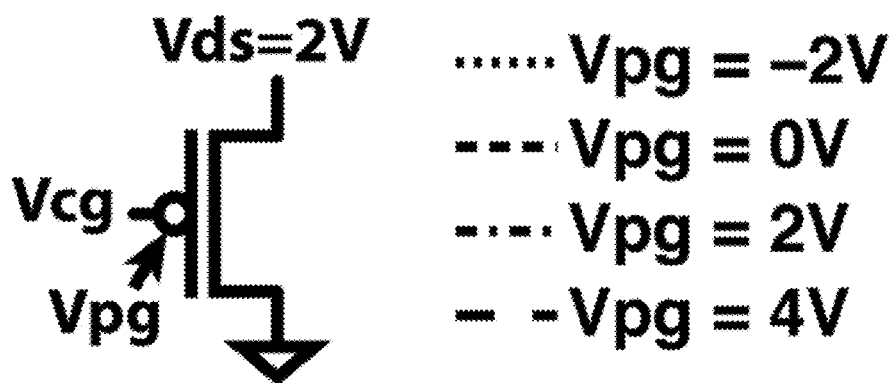


Fig. 5B

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# AMBIPOLAR SILICON NANOWIRE FIELD EFFECT TRANSISTOR

## FIELD OF INVENTION

The present invention relates to silicon nanowire field effect transistors (SNWFETs) and more precisely to new SNWFET architectures and processes for manufacturing such architectures.

## BACKGROUND

Bulk CMOS technologies are predicted to face crucial technological challenges in the next decade. At the same time, novel devices such as Carbon Nanotube Field Effect Transistors (CNTFETs) and Silicon Nanowire Field Effect Transistors (SNWFETs), which do not suffer from the same constraints, are expected to play a primary role as devices in future ultra-large scale integration technologies.

The interest in these devices is motivated not only by their small size, but also their superior characteristics, such as quasi-ballistic transport, steep sub-threshold slopes and one-dimensional channel geometry. Channel geometry, specifically, plays a major role in the current efforts towards miniaturization of devices, with transistor manufacturers currently moving from planar bulk MOSFETs to fully depleted SOI and FinFETs. Fully depleted SOIs, in particular, exploit the presence of a buried oxide layer below the device channel to screen the drain electric field from interfering with the gate electric field, thus reducing short channel effects. Moreover, fully depleting the channel enhances the device switching speed by requiring less gate field to turn on the device. FinFETs are a further evolution of this concept, exploiting vertical fin-like device channels, which can fully deplete and can be controlled on three surfaces by the electric field. In order to obtain the best electrostatic control over the device channel, however, one-dimensional channel structures need to be implemented. These include semiconducting mono or polycrystalline nanowires and carbon nanotubes (CNTs).

Among the types of CNTFETs demonstrated in literature, double-gate ambipolar CNTFETs are four-terminal devices where a second gate terminal is added to control the device polarity [3]. These devices combine performance exceeding that of current scaled MOSFETs, with the possibility to control the device polarity by electrostatic doping of the nanotubes [1]. Nevertheless, CNTFETs, as well as catalyst-grown nanowires, require a bottom-up fabrication approach, where nanotubes/nanowires are first grown in dedicated furnaces and subsequently purified, selected and transferred on the final substrate. Bottom up approaches have not been successful in proposing a large-scale device integration method primarily due to the challenges in selecting and positioning channel elements on the final substrates.

## GENERAL DESCRIPTION OF THE INVENTION

The present invention encompasses, among other objects, an electronic device consisting of one—or more—vertically stacked gate-all-around silicon nanowire field effect transistor (SNWFET) with two independent gate electrodes. One of the two gate electrodes, acting on the central section of the transistor channel, controls on/off behavior of the channel. The second gate, acting on the regions in proximity to the source and the drain of the transistor, defines the polarity of the devices, i.e., p or n type. The electric field of the second gate acts either at the interface of the nanowire-to-source/drain region or anywhere in close proximity to the depleted

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region of the SiNW body, modulating the bending of the Schottky barriers at the contacts, eventually screening one type of charge carrier to pass through the channel of the transistor. This is achieved by controlling the majority carriers passing through the transistor channel by regulating the Schottky barrier thicknesses at the source and drain contacts.

The present invention also discloses a method of fabricating semiconducting channel field-effect transistors having controlled polarity (n or p-type) by means of a double gate structure including a control gate and an independent polarity gate electrode. In one embodiment, the method includes forming a device channel composed of a stack of horizontal semiconducting nanowires held between two pillar-like source and drain contacts in which the pillars may also be hollowed down to a given depth by dry or wet etching and the silicide formed so as to reach the bottom nanowire and reduce contact resistance. A gate-all-around structure is then formed covering the side regions of the channel, in proximity of the source and drain Schottky barriers, the gate constructions allowing to form a positive or a negative electric field potential distribution between the gate structure and either the interface between the SiNW channel and/or the region of the SiNW which is depleted by the presence of the Schottky barrier contact. In another embodiment, the gate structure utilized to influence the region at the Schottky barrier interface or the neighboring region influenced by the presence of the Schottky contact is effective only to a reduced portion of the mentioned regions. In yet another embodiment the gate affects only the region in proximity of the source, either totally or partially. Finally, a second gate structure is formed around the central region of the nanowire stack along the nanowire length. In another embodiment, one or more parallel vertical semiconducting nanowires form the device channel, and the gate structures surround the vertical nanowires and are grown horizontally. In another embodiment, a vertical semiconducting fin-like structure forms the device channel, and the gate structures surround the fin-like channel covering the three exposed surfaces: the two fin side surfaces and the top surface. In another embodiment, a graphene ribbon forms the device channel, and the gate structure covers the top surface of the ribbon, or both the bottom and top surfaces of the ribbon.

This structure differs from conventional independent double gate devices, such as the one described in [2], where the second gate acts on the same region of the transistor channel as the first gate. In the case of the conventional independent double gate devices, the second gate is mainly used to tune the threshold voltage of the device. This tuning can be advantageous to reduce power consumption or tune device speed at runtime. Threshold tuning can also be present in our invention by the fact that the electric field distribution generated by one gate also affects the electric field distribution of the other gate. In this case the achievement of a polarity control by a double independent gate structure can also imply a threshold tuning, whose effects can be amplified or reduced by engineering electric field distributions generated by the two gates. This has to do with both the geometry of the gate construction and the materials utilized for electric field isolation. Nonetheless, another embodiment of the invention is the threshold tuning of polarity-controlled devices, which is a direct consequence of mutual dependence of the electric field potentials generated by the two gates. However, the structures described in [2] have the only purpose of achieving threshold tuning but at the same time present technological disadvantages such as the precise alignment of the two gates at the sides of the channel, and their independent doping.



Regarding the different solutions, the ambipolar-controlled logic gates is amongst the most promising ones, thanks to the higher expressive logic power due to the polarity control as state variable [4]. The polarity control can be achieved in ambipolar devices by using a double independent gate (DIG) structure. A few examples can be found for DIG FETs based on carbon nanotubes [5], [6], graphene [7], semiconducting polymers and silicon nanowires (SiNWs) [8]. Nevertheless, very limited research has been done in terms of integrating of ambipolar-controlled devices with CMOS compatible top-down Si fabrication flow, which is crucial for large-scale systems integration. The inventors demonstrated a double independent gate configuration with SiNW and top-down fabrication flow as useful building block for ambipolar-controlled logic operation [9]. Moreover, using the structure proposed in the present invention, more efficient logic circuits are fabricated, as demonstrated by the authors in [10,11,13].

In another embodiment the invention is based on a top-down fabrication procedure, with the nanowires being formed by a single etching step [12]. This method enables fabrication of horizontal nanowires, which can be stacked one on top of each other to increase device sizing. Moreover, several parallel nanowires can be fabricated with this method, further expanding the functioning range of our devices in terms of maximum ON current and power.

The unique combination of the invention herein described and specifically with respect to the following points:

1. Top-Down fabrication flow

2. CMOS compatible fabrication flow

enables the use of the device physical properties for regular fabric tiles made of polarity-controlled gates in large arrays. Thus the use of polarity-controlled devices and, more in general, of the ambipolarity property as a state variable, is enabled for computation in large electronic circuits by our invention. In fact, repeatable and reliable arrays of polarity-controlled devices fabricated by either bottom-down fabrication processes or non-repeatable device structures cannot be utilized in applications where large arrays of ambipolar devices with two double independent gates and polarity control are needed, due to the strict requirements of signal consistency and signal integrity.

In a first aspect the invention provides a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel.

In a second aspect the invention provides a method for manufacturing a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not

affected by the presence of a Schottky barrier interface, namely a portion of the channel. The method comprises steps of forming the SiNW channel from horizontal semiconducting nanowires; forming a vertical stack composed of a number of horizontal nanowires ranging from 1 to about 1000, held between two pillar-like structures; forming an insulating layer on which a gate electrode is formed, covering the regions of the vertical stack composed of horizontal nanowires, in proximity of the source and drain contacts of the device; forming a second insulating layer on which a second gate electrode is formed, covering a center region of the vertical stack composed of horizontal nanowires; forming a metallic layer on the source and drain pillars and creating a silicide in proximity of side regions of the vertical stack composed of horizontal nanowires, and forming a metallic region close to the source and drain in which the pillars may also be hollowed down to a given depth by dry or wet etching and the silicide formed so as to reach the bottom nanowire and reduce contact resistance.

In a first preferred embodiment vertical stack composed of horizontal nanowires is isolated from the transistor substrate by a dielectric, such as a buried oxide (BOX) layer.

In a second preferred embodiment the vertical stack composed of horizontal nanowires is electrically connected to the substrate.

In a third aspect the invention provides a method for manufacturing a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel. The method comprises forming a vertical semiconducting structure, self sustaining or sustained by pillar like structures; Forming an insulating layer on which a gate electrode is formed, covering the side and top surfaces of the fin-like structure in proximity of the source and drain contacts of the device; forming a second insulating layer on which a second gate electrode is formed, covering the center region of the fin-like structure at the side and top surfaces; forming a metallic layer on the source and drain pillars or regions and creating a silicide in proximity of the side regions of the fin-like structure; and forming a metallic region close to the source and drain in which the pillars may also be hollowed down to a given depth by dry or wet etching and the silicide formed so as to reach the bottom of the fin and reduce contact resistance.

In a third preferred embodiment the fin-like structures are isolated from the transistor substrate by a dielectric, such as a buried oxide (BOX) layer.

In a fourth preferred embodiment the fin-like structures are electrically connected to the substrate.

In a fourth aspect the invention provides a method for manufacturing a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, comprising an interface region between the metal-to-semiconductor contact; and a depleted region in the

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semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel. The method comprises forming a horizontal or vertical graphene nanoribbon connected between two metallic source and drain contacts; forming an insulating layer on which a gate electrode is formed, covering one or both surfaces of the graphene ribbon in proximity of the source and drain contacts of the device; and forming a second insulating layer on which a second gate electrode is formed, covering the center region of the ribbon at one or both surfaces.

In a fifth preferred embodiment the channel is formed from at least one of: Si, SiGe, Ge, using a top-down fabrication method such as using a controlled Bosch process dry etching or an anisotropic vertical etch plus a selective Si/SiGe etch.

In a fifth aspect the invention provides a method for manufacturing a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel. The two gate dielectric layers are each formed from at least one of: SiO<sub>2</sub>, HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, TiON, TiSiON, HfSiO, HfSiON, AlSiO, AlSiON.

In a sixth preferred embodiment the method is with any stoichiometry of the described dielectric layers.

In a sixth aspect the invention provides a method for manufacturing a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel. The metallic layer of choice is comprised from at least one transition metal (e.g. Ni, Ti, Co, Mn, Pt, Pd, . . . ).

In a seventh aspect the invention provides a method for manufacturing a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface,

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namely a portion of the channel. The silicide is formed from at least one transition metal (e.g. NiSi, NiSi<sub>2</sub>, TiSi<sub>2</sub>, CoSi, PdSi<sub>2</sub>, PtSi, . . . ).

In an eighth aspect the invention provides top down fabrication of sea-of-gates topology with ambipolar devices relying on double independent gate architecture for customization of their functionality.

In a ninth aspect the invention provides use of a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel, as a basic tile for fabrication of a sea-of-gates topology.

In a tenth aspect the invention provides use of a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel. The electric field potential to modulate the regions of the SiNW channel affected by the presence of the Schottky barrier interface is partially affected by the electric field potential, which modulates the further regions of the semiconducting channel not affected by the presence of the Schottky barrier interface.

In an eleventh aspect the invention provides use of a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, that comprises an interface region between the metal-to-semiconductor contact; and a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky contact. The silicon nanowire field effect transistor further comprises a second gate structure utilized to produce an electric field potential, which modulates further regions of the semiconducting channel not affected by the presence of a Schottky barrier interface, namely a portion of the channel. The electric field potential, which modulates the further regions of the semiconducting channel not affected by the presence of the Schottky barrier interface is partially affected by the electric field potential to modulate the regions of the SiNW channel affected by the presence of the Schottky barrier interface.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be understood better in light of the detailed description and of the figures, wherein the following short introduction is given:

FIG. 1A: Process flow sequence for the fabrication of a Double Independent Gate structure;

FIG. 1B: Schematic symbol of a double independent gate polarity-controlled transistor;

FIG. 1C: A double independent gate structure with 1 SiNW channel;

FIG. 1D: A double independent gate structure with 4 vertically stacked SiNW channels;

FIG. 2A: Top View of the SiNW channels anchored between two Si pillars;

FIG. 2B: Side View of the SiNW channels anchored between two Si pillars;

FIG. 2C: Top View of the first gate overlapping the regions in close proximity of the Si pillars. Later in the process the regions surrounded by this gate will be those mostly affected by the presence of a Schottky barrier (typically but not exclusively at the anchor point between SiNW and Si pillars);

FIG. 2D: Side View of the first gate overlapping the regions in close proximity of the Si pillars. Later in the process the regions surrounded by this gate will be those mostly affected by the presence of a Schottky barrier (typically but not exclusively at the anchor point between SiNW and Si pillars);

FIG. 2E: Top View of the structure after the second gate is patterned. The second gate is placed in the central region of the SiNW channels;

FIG. 2F: Side View of the structure after the second gate is patterned. The second gate is placed in the central region of the SiNW channels;

FIG. 2G: Top View of the structure after the sidewall spacer is defined. The sidewall spacer covers all the steps of the structure, thus providing isolation between the different parts;

FIG. 2H: Side View of the structure after the sidewall spacer is defined. The sidewall spacer covers all the steps of the structure, thus providing isolation between the different parts;

FIG. 2I: Top View of the structure after the deposition of a suitable metal for the silicide process;

FIG. 2J: Side View of the structure after the deposition of a suitable metal for the silicide process;

FIG. 2K: Top View of the structure after silicide formation;

FIG. 2L: Side View of the structure after silicide formation;

FIGS. 3A-3F: A 2<sup>nd</sup> example of fabrication flow for double independent gate with Si nanowire structure in particular:

FIG. 3A: Top view of the dual gate device. The next steps focuses on the double independent gate area construction;

FIG. 3B: Photoresist mask is patterned;

FIG. 3C: After isotropic etching of Si a triangular-shaped SiNW is formed;

FIG. 3D: Gate oxidation and LPCVD polysilicon are deposited and patterned to form the main, central gate stack;

FIG. 3E: A low temperature oxide (LTO) inter-poly dielectric is deposited and a second polysilicon gate is made self-aligned with the nanowire;

FIG. 3F: Focused ion beam cross-section showing a triangular SiNW channel with two 75 nm sides and 100 nm base. The gate1, gate2 and the LTO inter-poly dielectric have 150 nm, 500 nm and 300 nm thicknesses, respectively. Gate1 dielectric is 30 nm thick;

FIGS. 4A-4M: A 3<sup>rd</sup> example of fabrication flow for double independent gate structure with SiNW channel in particular:

FIG. 4A: 3D View of a double independent gate structure with vertical Si nanowire channel;

FIG. 4B: Side View of a SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> hard mask patterned on top of the SOI device layer;

FIG. 4C: Side View of a vertical Si nanowire etched in the SOI device layer. A residual Si layer is left;

FIG. 4D: Side View of a vertical Si nanowire surrounded by a SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub> spacer;

FIG. 4E: Side View of a vertical Si nanowire surrounded by a SiO<sub>2</sub> or a Si<sub>3</sub>N<sub>4</sub> spacer after the patterning of the residual Si layer;

FIG. 4F: Side View of the vertical Si nanowire structure after NiSi formation and excess Ni etch by a hot Piranha solution;

FIG. 4G: Side View of the vertical Si nanowire structure after high-k dielectric replacement and TiN electrode patterning;

FIG. 4H: Side View of the vertical Si nanowire structure after the first gate is patterned;

FIG. 4I: Side View of the vertical Si nanowire structure after the first gate is patterned on the high-k/TiN samples;

FIG. 4J: Side View of the vertical Si nanowire structure after the second gate is patterned;

FIG. 4K: Side View of the vertical Si nanowire structure after the second gate is patterned on the high-k/TiN samples;

FIG. 4L: Side View of the vertical Si nanowire structure after the first gate is extended in the region close to the top NiSi contact;

FIG. 4M: Side View of the vertical Si nanowire structure after the first gate is extended in the region close to the top NiSi contact on the high-k/TiN samples;

FIG. 5A: n- and p-type conduction is selected by different V<sub>pg</sub> (second gate voltage) biases. Currents in the p-type and n-type branch are comparable. Both n and p-type device branches show subthreshold slopes of about 70 mV/dec. Ion/I<sub>off</sub> ratios of about 10<sup>7</sup> (10<sup>6</sup>) are obtained respectively for the n-type (p-type) conduction branches. This curve demonstrate the feasibility of the polarity control, full explanation can be found in reference [13]; and

FIG. 5B: The device connections and voltage biases are referring to the measurements of FIG. 5A [13].

## DETAILED DESCRIPTION OF THE INVENTION

Three non-limiting examples of processes, which can be used with the present invention, are presented below.

### 1ST EXAMPLE

In a 1<sup>st</sup> example, the main steps of the device fabrication procedure are listed in FIG. 1A. Generally, the process includes creating a device channel, that is, a transistor channel 1 (FIG. 2J below), which can be composed of a vertical stack of a variable number of horizontal semiconducting nanowires, a parallel array of vertical stacks of horizontal nanowires, a fin-like structure (from which a FinFET transistor would be obtained) or a graphene ribbon. We will use the nanowire stack further on in this description as an example. FIG. 2B shows a cross section of the nanowire stack, with two pillar-like structures sustaining the nanowires, while FIG. 2A shows the top view of such stack.

After the channel structure is fabricated, a first gate insulator covering the channel section of the transistor is created. This gate insulator can be produced by direct oxidation of the transistor channel, or by deposition of various high-k dielectric materials.

A 1st gate electrode is deposited over the 1st gate insulator, and patterned to obtain a gate structure covering the side regions of the transistor channel (FIGS. 2C and 2D). This 1st gate structure will approach or partly overlap the regions where source/drain contacts will be formed.

After the first gate electrode is fabricated, a second gate insulator is created in order to isolate the center region of the

device, and a second gate electrode is deposited and patterned to act on the central region of the device. This second gate can be created by self-alignment to the 1<sup>st</sup> gate electrode (FIGS. 2E and 2F).

After the second gate is formed, a spacer is formed by deposition and etching of a dielectric material such as Silicon Nitride (FIGS. 2G and 2H), in order to isolate gate electrodes and source/drain regions further on, when contacts will be formed.

Finally, an interface region 2 of the device is covered with a metal exhibiting near mid-gap work-function with respect to the channel semiconductor material (FIGS. 2I and 2J. By annealing, a silicide can be formed to create desired a Schottky barrier interface 3 at the two sides of the device channel, that is, the transistor channel 1, so that source/drain Schottky barriers approach or are covered by the first gate electrode (FIGS. 2K and 2L).

## 2ND EXAMPLE

In a 2<sup>nd</sup> example, a single Si nanowire with Double Independent Gates, that is, Schottky barrier interfaces 4, is fabricated (see Top View of FIG. 3A). A low doping p-type ( $N_A \sim 10^{15}$  atoms/cm<sup>2</sup>) SOI wafer with 1.5  $\mu$ m device layer is spin coated. The photoresist is then patterned in 1.5  $\mu$ m wide lines (see FIG. 3B) and used as mask for a next isotropic Si etching. A Si plasma etching recipe is tuned to form a triangular 75 nm wide Si nanowire lying on top of the buried oxide (BOX) layer (FIG. 3C). The Si nanowire is a transistor channel 5 in this embodiment. Then a 30 nm thick gate oxidation and a 150 nm polysilicon layer are deposited with a low-pressure chemical vapor deposition (LPCVD) method to form a main gate with 7.5  $\mu$ m length (gate 1, FIG. 3D). 300 nm LPCVD low temperature oxide (LTO) is used to isolate the main gate. A second 500 nm polysilicon layer is then deposited. Then a thick photoresist is spun over the wafer and planarized using a chemical mechanical polishing procedure. This method leaves a protective polymer layer that is used to etch a second polysilicon gate self-aligned within the cavity thanks to the topography (see gate 2 in FIG. 3E). After standard cleaning steps, one additional patterning of gate 2 is performed to remove the unnecessary polysilicon and to form areas for the contacts (see the top view of the device in FIG. 3A). In FIG. 3F a focused ion beam cross-section of the triangular SiNW channel, that is, a depleted region 6, with the double independent gate stack is shown. Then source/drain contacts are formed by means of NiSi silicidation in a horizontal wall furnace in forming gas at 400° C. Finally Al metal lines and pad area are defined for the electrical characterization.

## 3RD EXAMPLE

In a 3<sup>rd</sup> example, vertical Si nanowires with Double Independent Gate All-Around are fabricated (see FIG. 4A). The Si nanowires are vertically etched in parallel on 10 SOI wafers after having patterned a SiO<sub>2</sub> hard mask by lithography (FIG. 4B and FIG. 4C). The Si nanowire are then freestanding and anchored at the bottom where a Si layer is still left for subsequent processing (FIG. 4C). Then a SiO<sub>2</sub> or a Si<sub>3</sub>N<sub>4</sub> layer is deposited all-around by LPCVD method on 9 and 1 SOI wafer, respectively. Then SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> spacers are formed by vertical plasma etching in a dry etching tool (FIG. 4D). At this stage, the Si nanowires are surrounded by a SiO<sub>2</sub> or a Si<sub>3</sub>N<sub>4</sub> dielectric, while the planar layer on top of the Buried Oxide and the top section of the Si nanowires reveal a non-passivated Si surface or with a native Si oxide thinner than 10

angstroms. Then another lithography defines the bottom layer that is etched in order to isolate the Si nanowires (FIG. 4E). Subsequently, a Ni metal layer is deposited by electron beam evaporation and annealed at 450° C. in a Rapid Thermal Annealing furnace with constant N<sub>2</sub> flow for 20 seconds. The annealing process is carried out in order to form a thin NiSi layer at the top and at the bottom of the Si nanowires; thus Ni alloys with Si due to the contact with Si. For the Si regions masked by the thick SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub> spacer, the Ni metal cannot react with Si. The sample is then dipped into a hot Piranha solution in order to strip the unreacted Ni layer, leaving only the NiSi Schottky barrier interface 7 and the Si nanowire, that is, the depleted region 8, structure surrounded by the dielectric mask, thanks to the etching selectivity between Ni and NiSi, Si, SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub> in hot Piranha solution (see FIG. 4F). For 8 SOI wafers the SiO<sub>2</sub> surrounding the Si nanowire is stripped by vapor HF method and replaced by one of the following high-k dielectrics, one per each SOI wafer:

1. HfO<sub>2</sub>;
2. TiO<sub>2</sub>;
3. Al<sub>2</sub>O<sub>3</sub>;
4. ZrO<sub>2</sub>;
5. HfSiO;
6. HfSiON;
7. Ta<sub>2</sub>O<sub>5</sub>;
8. Lead-zirconate-titanate (PZT);

All the high-k dielectrics are deposited by atomic layer deposition (ALD) system. Subsequently to the high-k dielectric deposition, a 10 nm thin TiN is deposited in the same ALD equipment without breaking the vacuum. Then the high-k samples are processed in a conventional dry etcher tool in order to remove the high-k material and the TiN on top of the NiSi regions (FIG. 4G). A transistor channel 9 is formed.

Then all the 10 SOI wafers are covered by a 50 nm thick amorphous Si layer deposited by LPCVD followed by a spin coating of a 50 nm thick HSQ layer. After the HSQ exposure in an e-beam lithography system, excessive amorphous Si is etched isotropically in a dry etcher with a SF<sub>6</sub>/C<sub>4</sub>F<sub>8</sub> plasma with low bias to minimize ion bombardment and maximize the chemical reaction between SF<sub>6</sub> ions with the amorphous Si. At this stage a first amorphous Si gate surrounds the Si nanowire portion close to the bottom NiSi contact (see FIG. 4H for SiO<sub>2</sub> or Si<sub>3</sub>N<sub>4</sub> dielectrics and FIG. 4I for high-k dielectrics). Then the amorphous Si deposition step and HSQ lithography are repeated in order to define a second independent gate (see FIG. 4J for SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> and FIG. 4K for the high-k/TiN stack). Then another layer of amorphous Si is deposited after capping the second independent gate with a dielectric. In this way the first gate is extended to the region in proximity of the top NiSi to SiNW contact (see FIG. 4L for SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> and FIG. 4M for the high-k/TiN stack).

The TiN in the high-k samples is then removed by dipping into a RCA1 chemical solution at 60° C. for 60 s, thus isolating the two gates and the NiSi contacts.

Then, the Si nanowire structures are passivated in a Low Temperature Oxide matrix deposited by LPCVD and VIA holes are etched on top of the NiSi contacts and the gate vias. Finally, Chemical Mechanical Polishing and lift-off are used respectively to define W plugs and Al wires.

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The invention claimed is:

1. A method for manufacturing a silicon nanowire (SiNW) field effect transistor device with a double independent gate structure, the silicon nanowire field effect transistor comprising:
  - a first gate used to build up an electric field potential to modulate regions of a SiNW channel affected by a presence of a Schottky barrier interface, comprising:
    - an interface region between the metal-to-semiconductor contact; and
    - a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky barrier interface;
- the silicon nanowire field effect transistor further comprising:

a second gate structure utilized to produce an electric field potential, which modulates further regions of a semiconducting channel not affected by the presence of the Schottky barrier interface, namely a portion of the channel

the method comprising;

forming the SiNW channel as a vertical semiconducting fin-like structure, self sustaining or sustained by pillar like structures, one of the pillar like structures embodying a drain contact, another of the pillar like structures embodying a source contact;

forming an insulating layer on which the first gate electrode is formed, covering side and top surfaces of the fin-like structure in proximity of the source and drain contacts; forming a second insulating layer on which the second gate electrode is formed, covering a center region of the fin-like structure at the side and top surfaces;

forming a metallic layer on the pillars embodying the drain and source contact respectively and creating a silicide in proximity of the side regions of the fin-like structure; and

forming a metallic region close to the source and drain in which the pillars may also be hollowed down to a given depth by dry or wet etching and the silicide formed so as to reach the bottom of the fin and reduce contact resistance.

2. The method of claim 1, wherein the vertical semiconducting fin-like structure comprises horizontal semiconducting nanowires in a vertical stack composed of a number of horizontal nanowires ranging from 1 to about 1000, held between the pillars embodying the drain and source contacts respectively.

3. The method of claim 1, wherein the fin-like structures are isolated from the transistor substrate by a dielectric, such as a buried oxide (BOX) layer.

4. The method of claim 1, wherein the fin-like structures are electrically connected to the substrate.

5. A method for manufacturing a graphene nanowire field effect transistor device with a double independent gate structure, the graphene nanowire field effect transistor comprising:

a first gate used to build up an electric field potential to modulate regions of a graphene channel affected by a presence of a Schottky barrier interface, comprising:

an interface region between the metal-to-semiconductor contact; and

a depleted region in the semiconductor whose depletion is consequence of the presence of the Schottky barrier interface;

the graphene nanowire field effect transistor further comprising:

a second gate structure utilized to produce an electric field potential, which modulates further regions of a semiconducting channel not affected by the presence of the Schottky barrier interface, namely a portion of the channel;

the method comprising:

forming a horizontal or vertical graphene nanoribbon connected between two metallic source and drain contacts, the graphene nanoribbon comprising the graphene nanowire;

forming an insulating layer on which the first gate electrode is formed, covering one or both surfaces of the graphene nanoribbon in proximity of the source and drain contacts; and

forming a second insulating layer on which the second gate electrode is formed, covering the center region of the graphene nanoribbon at one or both surfaces.

6. The method of claim 1 wherein the SiNW channel is formed from at least one of: Si, SiGe, Ge, using a top-down fabrication method such as using a controlled Bosch process dry etching or an anisotropic vertical etch plus a selective Si/SiGe etch.

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7. The method of claim 1,

wherein dielectric layers of the first gate and of the second gate are each formed from at least one of: SiO<sub>2</sub>, HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, TiON, TiSiON, HfSiO, HfSiON, AlSiO, AlSiON.

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8. The method of claim 7 with any stoichiometry of the claimed dielectric layers.

9. The method of claim 1,

wherein the metallic layer is comprised from at least one transition metal (e.g. Ni, Ti, Co, Mn, Pt, Pd, . . . ).

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10. The method of claim 1,

wherein the silicide is formed from at least one transition metal (e.g. NiSi, NiSi<sub>2</sub>, TiSi<sub>2</sub>, CoSi, PdSi<sub>2</sub>, PtSi, . . . ).

11. The method of claim 1, wherein the method implements top down fabrication of sea-of-gates topology with ambipolar devices relying on double independent gate architecture for customization of their functionality.

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12. The method of claim 5, wherein the method implements top down fabrication of sea-of-gates topology with ambipolar devices relying on double independent gate architecture for customization of their functionality.

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